REMARKS

In accordance with the foregoing, claims 1 and 9 have been amended. Claims 17-19 have been added. Thus, claims 1-5, 7-13 and 15-19 are pending and under consideration.

35 U.S.C. § 102(e) Rejections

In item 2, spanning pages 2-3 of the July 19, 2005 Office Action, claims 1-5, 7-13 and 15-16 were rejected under 35 U.S.C. § 102(e) as being anticipated by Lai et al. (US Patent 6,216,193) (hereafter "Lai"). The rejections are respectfully traversed.

As amended, claim 1 recites: "a data holding part which holds data at a time when said interrupt starts to occur, said data holding part holding data for continuing an instruction that is not a cause of said interrupt and that is interrupted due to occurrence of said interrupt" (claim 1, lines 3-5) and described in the specification at least at page 16, lines 32-37; page 17, lines 1-5; page 17, lines 36-37; page 18, lines 1-5; page 19, lines 4-13; page 28, lines 1-14; and page 32, lines 26-33. In other words, in Applicants' invention, when an interrupt starts to occur, data processing at that time is held in memory so that processing of that data can be continued without repeating (i.e., reloading) an instruction after the interrupt is discontinued.

In contrast, what was cited in Lai describes "if the PCI (peripheral component interconnect) bus transfer is interrupted, the reload address is supplied to the random access buffer memory to enable data output holding registers to be reloaded with the data lost by the target during the interrupted DMA transfer" (ABSTRACT); data lost during a PCI burst transfer can be recovered merely by supplying the reload address to the memory ... and the address holding register" (column 7, lines 12-32); "the target interrupts the PCI transfer by deasserting the target ready signal ... and asserting the stop signal ... causing the output holding register ... to hold the data set ... on [the] PCI bus" (column 12, lines 16-22). In other words, if the PCI bus transfer is interrupted, the reload address in the reload address register is supplied to the random access buffer memory to enable data output holding registers to be reloaded with the data lost by the target during the interrupted DMA transfer. The reload address register is incremented based on the target successfully receiving a data word. However this differs from Applicants' invention because, Lai does not suggest holding data for continuing an instruction that is not a cause of the interrupt and that is interrupted due to the occurrence of the interrupt. Lai merely describes recovering lost data in a DMA data transfer that causes the transfer interrupt. Thus, claim 1 is not anticipated by Lai and is in condition suitable for allowance.

Claim 9 recites interrupt limitations in a manner similar to claim 1; and claims 2-5, 7-8, 10-13 and 15-16 depend from claims 1 and 9; thus, claim 9 and claims 2-5, 7-8, 10-13 and 15-16 patentably distinguishe over Lai for the same reasons discussed in regard to claim 1.

NEW CLIAMS

Newly added claims 17-19 further clarify the distinctions of the present invention over the applied art. Specifically claim 17 recites: "holding in a memory at least an address of an instruction in an operation when interrupt processing that is not caused by the instruction causes the operation to halt" (claim 17, lines 2-3), as described in the specification at least at page 16, lines 32-37 and page 17, lines 1-5. Nothing has been cited or found in Lai that shows the limitations of claim 17. Lai merely describes establishing recovery processing of lost data after an interrupt condition.

Dependent claims 18 and 19 which depend from claim 17 patentably distinguish over the applied art for the reasons discussed in regard to claim 17.

In addition, nothing has been cited or found in Lai that shows "continuing the operation by executing the instruction held in the memory after the interrupt processing is discontinued" (claim 18, lines 2-3). In other words, nothing has been found in Lai that shows after the interrupt condition, restarting the halted operation where it stopped, based on the address of the operation instruction held in memory. In regard to claim 19, nothing has been cited or found in Lai that shows "said address of an instruction is held in the memory when the interrupt processing starts to occur" (claim 19, lines 1-3). In other words, nothing has been found in Lai that shows holding an address of an operation instruction in a memory when the interrupt processing is initiated. As discussed above, Lai merely describes establishing recovery processing of lost data after an interrupt condition.

CONCLUSION

It is submitted that the reference cited in the July 19, 2005 Office Action does not teach or suggest the features of the present claimed invention as amended and for the reasons presented above, Applicants' invention is not anticipated. There being no further outstanding objections or rejections, it is submitted that claims 1-5, 7-13 and 15-19 are in condition suitable for allowance. An early action to that effect is courteously solicited.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

Finally if there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450
on November 21, 2005
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